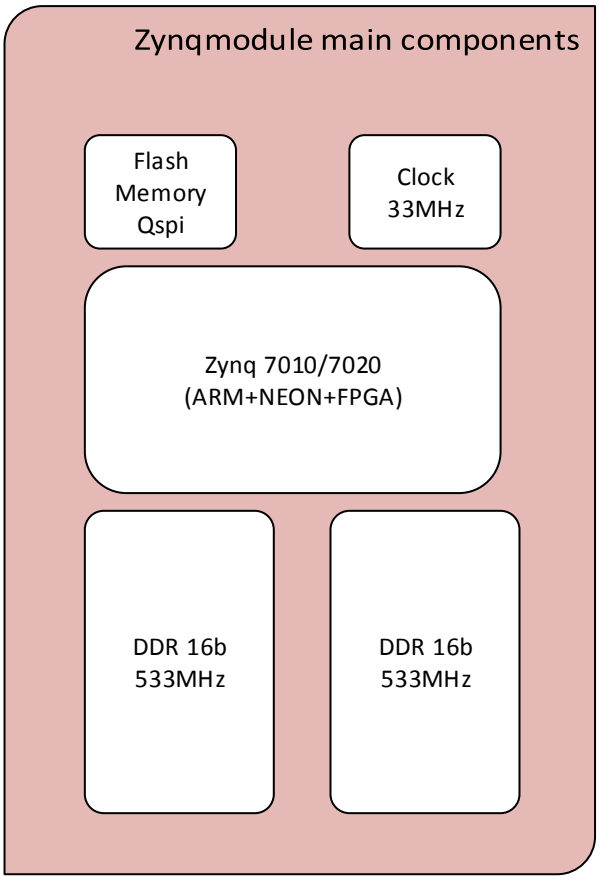
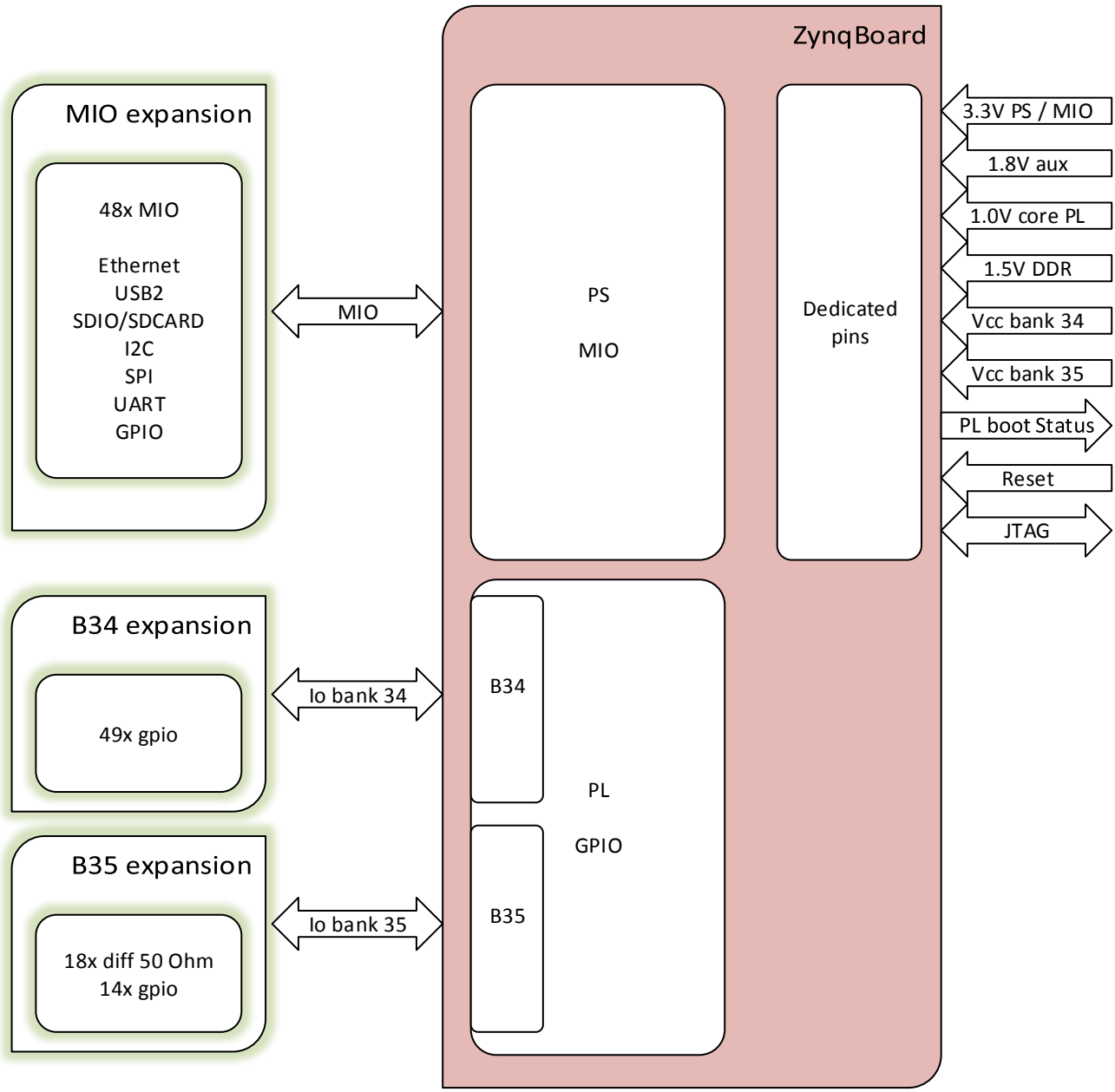

Zynqmodule main components
Flash
Memory
Qspi
Clock
33MHz
Zynq 7010/7020
(ARM+NEON+FPGA)
DDR 16b
533MHz
DDR 16b
533MHz



Each diff signal can also be use as two single ended signals

MIO is connected to the Processor System (PS) and can be setup to a variety of functions, like Ethernet, USB, SDIO, I2C, GPIO etc.